NEWPORT

2001
DIGITAL PANEL VOLTMETER

10546ML-02

Electronic Services - Los Angeles
M13634X

OWNERS MANUAL

2.0 SPECIFICATIONS

2.1 ANALOG INPUT

Model 2001	-3	-4	-5
Range	±1.9999 V dc	±19.999 V dc	±199.99 V dc
Resolution	0.1 mV	1 mV	10 mV
Maximum input	250 V rms, 350 Vp	750 V rms, 1000 Vp	750 V rms, 1000 Vp
Input resistance	1 GΩ 1 MΩ	1 MΩ	
Bias current	10 pA 1 pA	1 pA	
Configuration		differential	
Zero		automatic	
Span adjustment		±5%	

Model 2001-AC	-AC5	-AC6
Range	±199.99 V ac	650.0 V ac
Resolution	10 mV	100 mV
Maximum input	750 V rms, 1000 Vp	750 V rms, 1000 Vp
Input resistance	1 MΩ	1 MΩ
Bias current	1 pA	1 pA
Configuration	half-wave average, rms-calibrated	
Zero	automatic	
Frequency	49-440 Hz	

2.2 REFERENCE INPUT FOR 3-WIRE RATIO

Analog input range	±2 V dc, ±20 V dc, ±200 V dc
Reference voltage	+0.5 to +2.0 V
Load on reference	80 Ω (std), 100 MΩ (opt)
Accuracy	99.98%

2.3 NOISE REJECTION

NMR, sig hi to sig lo	56 dB at 50/60 Hz
CMR, sig lo to ana gnd	86 dB from DC to 60 Hz
CMV, sig lo to ana gnd	±1.0 V dc
CMR, ac gnd to ana gnd	120 dB from DC to 60 Hz
CMV, ac gnd tq ana gnd	2100 Vp per HV test, 354 Vp per IEC 348 spacing

2.4 ACCURACY AT 25°C

Maximum error	
2001	±0.01% of reading ±2 counts
2001-AC (20.00 to 199.99 V ac)	0.005%FS(R-110V)/ V ±2 counts
2001-AC (20.0 to 650.0 V ac range)	0.0005%FS(R-330V)/ V ±2 counts
Span tempco	±0.01% of reading/°C
Step response 2001, 2001-AC	1 second, 10 seconds
Warmup to rated accuracy	10 minutes

2.5 DIGITAL INPUTS

Positive true referenced to DIG GND

Input:	Logical 0	Logical 1	Sink	Source
$\overline{\text{HOLD}}$	0 to 0.8 V	2.8 to 5.0 V	0.1 mA	10 uA
$\overline{\text{LAMP TEST}}$	0 to 0.6 V	2.0 to 5.0 V	1.3 mA	20 uA
DISPLAY $\overline{\text{BLANKING}}$	0 to 0.6 V	2.0 to 5.0 V	1.3 mA	20 uA

2.6 ANALOG-TO-DIGITAL CONVERSION

Technique	Dual-slope, average-value
Input integration period	100 milliseconds
Read rate	2.5/second

2.7 DISPLAY

Digit type	7 segments, 14.2 mm (0.56 in) height
Symbols	-1.8.8.8.8
Decimal Points	4 positions, programmable internally or at the rear connector
Overrange indication	4 least-significant digits flash

2.8 POWER

Standard AC power voltage	115 or 230 V ac ±15%
AC frequency range	49 to 440 Hz
Optional DC power voltage	9-32 or 26-56 V dc, isolated to 300 Vp
Power consumption	2.4 W
Output voltages	+4.7 V dc ±5% at 10 mA max - 4.6 V dc ±5% at 10 mA max

4.0 POWER AND SIGNAL

AC versions of the 2001 and 2001-AC are factory-set for 115 V ac in the USA and 230 V ac in Europe (using C1 option) ±15% operation. DC versions are preset for 9-32 V dc or 26-56 V dc operation. It is not possible to change the meter from 9-32 V dc to 26-56 V dc or vice versa. Different static inverters are installed by Newport or its distributors.

Refer to Safety Considerations in Section 3 prior to connecting power.

4.1 CHANGING OPERATING VOLTAGE

Remove power lines from the meter, then remove the meter from the case.

OPERATING VOLTAGE	JUMPER INSTALLATION
230 V ac ±15% (Option C1)	Remove W8 and W9 *on the transformer* Install W4 *on the printed circuit board*
115 V ac ±15% (Standard)	Install W8 and W9 *on the transformer* Remove W4 *on the printed circuit board*

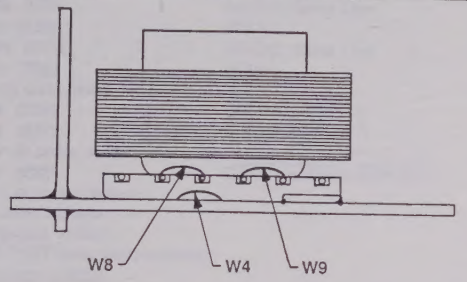


Figure 4-1
Side View of Transformer

4.2 POWER AND SIGNAL CONNECTIONS

Use shielded, twisted cable for the input signal, with the shield terminated to analog ground at the connector. Both analog and digital ground are internally connected and should not be connected externally. For proper grounding, connect the low signal to SIG LO *(signal low)*.

A jumper at S3-A (Figure 5-2 Main Board) ties SIG LO to ANA GND *(analog ground)* internally. The common for digital inputs/outputs is connected to DIG GND *(digital ground)*. This allows current to flow only in the digital ground and prevents IR drop in the analog ground that would be misread as a signal. A small voltage may exist between analog and digital grounds on connector J1.

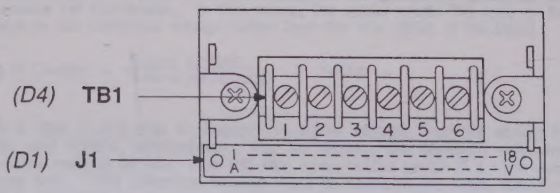


Figure 4-2
Rear Terminal Hookups

MODEL 2001

		POWER		SIGNAL	
AC	D1 Connector	A	High	17	High
		2	Low	16	Low
		C	Earth Ground	T	Analog Ground
	D4 Connector	1	High	6	High
		2	Low	5	Low
		3	Earth Ground	4	Analog Ground
DC	D1 Connector	2	+ DC	17	High
		C	- DC (return)	16	Low
				T	Analog Ground
	D4 Connector	2	+ DC	6	High
		3	- DC (return)	5	Low
				4	Analog Ground

MODEL 2001-AC

	D4 Connector	1	High	6	High
		2	Low	5	Low
		3	Earth Ground	4	Analog Ground

Wire Color for AC Power	*USA*	*Other*
(High)	*Black*	*Brown*
(Low)	*White*	*Blue*
(Ground)	*Green*	*Green*

4.3 MAIN BOARD PIN ASSIGNMENTS (J1 Card Edge)

Left to right, looking at rear of case

P1 Connection	Standard	With Serial BCD (F7 option)
A	Spare (E16)	Same function as standard unless specified below.
1	No connection	
B	No connection	
2	Spare (E18)	
C	Spare (E19)	
3	No connection	
D	No connection	
4	No connection	
E	Spare	D1-Digit Select Line
5	No connection	
F	1999.9 (DP4)	D2-Digit Select Line
6	Spare (E24)	BCD1
H	199.99 (DP3)	D3-Digit Select Line
7	Spare (E23)	BCD2
J	19.999 (DP2)	D4-Digit Select Line
8	Spare (E22)	BCD4
K	1.9999 (DP1)	D5-Digit Select Line
9	Spare (E25)	BCD8
L	Decimal point select	
10	Spare (E26)	OVERRANGE
M	Spare (E27)	+ POLARITY
11	-4.6 V dc power output	
N	Spare (E29)	DATA READY or $\overline{\text{STROBE}}$
12	+4.7 V dc power output	
P	- Excitation voltage	
13	+ Reference voltage	
R	$\overline{\text{LAMP TEST}}$ (lights display segments)	
14	+ Excitation voltage	
S	Digital ground	
15	$\overline{\text{HOLD}}$ (holds last display reading)	
T	Analog ground	
16	Spare (E32)	
U	$\overline{\text{BLANKING}}$ (blanks four least-significant-digits)	
17	Spare (E34)	
V	Oscillator (100 kHz output)	
18	No connection	

4.4 SIGNAL INPUTS

RATIO: The reference input allows an external voltage to be used as the reference source for conversion. In this mode, the meter reads the ratio of the signal voltage to the reference voltage rather than the true value of the input.

$$\text{Reading in Counts} = \frac{\text{Signal Voltage}}{\text{Reference Voltage}} \times 10000$$

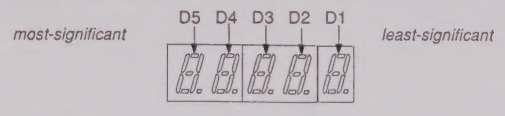
On the 20 V, 200 V and 650 V ranges, the signal voltage must be scaled by 1/10, 1/100, and 1/1000, respectively. For all ranges, the standard reference input impedance ratio is 80 MΩ. For 100 MΩ, open solder switch F on the main board (Figure 5-3). The reference voltage must be between the limits specified, +.5 to +2.0 V, and must be positive with respect to analog ground.

$\overline{\text{HOLD}}$: When high (or open), the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will complete the full measurement cycle and then hold this reading as long as $\overline{\text{HOLD}}$ is low. A positive pulse (greater than 300 ns) will now initiate a new measurement cycle, beginning with between 9,001 and 10,001 counts of auto-zero time. If the pulse terminates before the full measurement cycle (40,002 counts) is complete, it will not be recognized and the converter will simply complete the present measurement. An external indication that a full measurement cycle has been completed is that the first strobe pulse will occur 101 counts after the end of this cycle. Thus, if $\overline{\text{HOLD}}$ has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

$\overline{\text{BLANKING}}$: The display may be blanked by grounding the $\overline{\text{BLANKING}}$ input. The blanking input must be open for normal display operation. The polarity sign and decimal points are not blanked, but they will flash if the displayed reading exceeds ±19999 counts.

4.5 SIGNAL OUTPUTS

DIGIT DRIVES: Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D5 (MSD), D4, D3, D2, and D1 (LSD). All five digits are scanned and this scan is continuous unless an overrange occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference integrate when D5 will start the scan again. This can give a blinking display as a visual indication of overrange.



BCD: Used in the serial BCD option F7, the binary coded decimal bits BCD8, BCD4, BCD2, and BCD1 are positive true logic signals that serially represent the BCD digit corresponding to each digit drive signal.

OVERRANGE: Used in the serial BCD option F7, this signal goes positive when the input signal exceeds the range (20,000 counts) of the meter. The output flip-flop is set when DATA READY goes true and is reset at the beginning of reference integrate in the next measurement cycle.

+POLARITY: Used in the serial BCD option F7, this signal is positive for a positive input signal and is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least-significant bit. This output becomes valid at the beginning of reference integrate and remains correct until it becomes valid for the next measurement.

$\overline{\text{DATA READY}}$: Used in the serial BCD option F7, this signal goes high (false) at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse and are latched at the end of this clock pulse.

$\overline{\text{STROBE}}$: Used in the parallel BCD option F2N, this signal is a negative-going output pulse that aids in transferring the BCD data to external latches, UARTs or micro-processors. There are 5 negative-going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once (only) for each reading starting 101 pulses after the end of the full measurement cycle. Digit 5 (most-significant) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid a race condition between changing BCD and digit drive outputs), the first $\overline{\text{STROBE}}$ pulse goes negative for 5 microseconds. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (least-significant) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

5.0 CONFIGURATION

Select the desired configurations from the following charts. Install jumpers and open/close solder switches as indicated. Remove all push-on jumpers not used.

5.1 DECIMAL POINT SELECTION

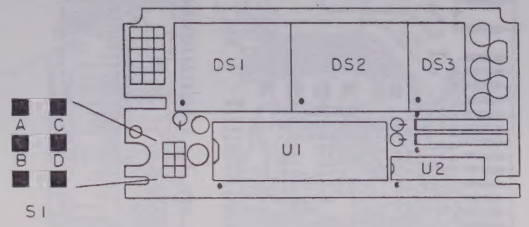


Figure 5-1 Display Board Jumper Locations

Decimal Point	S1	Alternate decimal point configuration using main board connector J1.
1.9999	A	Connect K to L
19.999	C	Connect J to L
199.99	B	Connect H to L
1999.9	B	Connect H to L

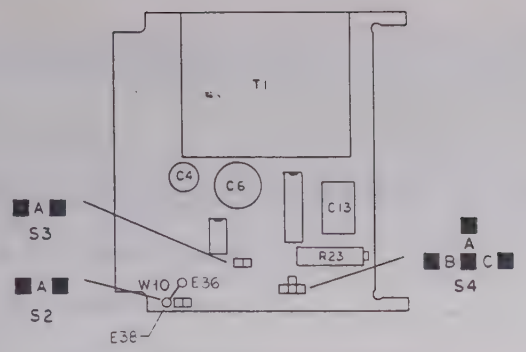


Figure 5-2 Main Board Jumper Locations

Input Configuration	Solder Switches *		Push-on Jumpers		Wire Jumper
	Open	Close	S2	S4	W10
2 V dc	J, L	H, I, K	-	-	Install
20 V dc	J, L	H, I, K	A	B	Remove
200 V dc	J, L	H, I, K	A	C	Remove
200 V ac	H, I, K	J, L	A	C	Remove
650 V ac	H, I, K	J, L	A	A	Remove

* Refer to Figure 5-3.

S3-A is used for signal connections. Refer to Section 4 for more information.

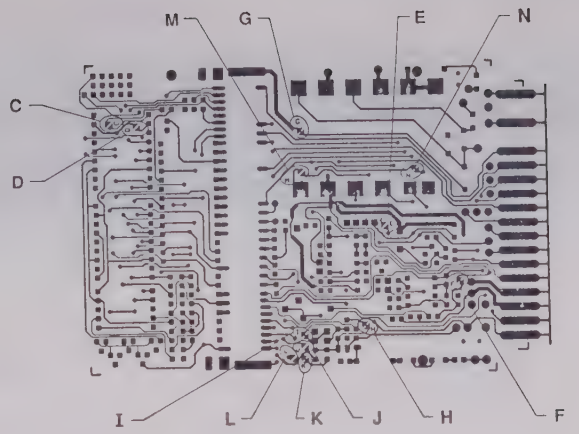


Figure 5-3 Solder Switch Locations

NOTE: Solder switch F is used for reference input impedance ratio. Refer to Section 4 for more information.

6.0 CALIBRATION

This unit was factory-calibrated with a precision voltage source. Frequent calibration is not necessary due to the stability and internal accuracy. If calibration is needed, use the following procedure.

6.1 DC VOLTAGE RANGES

1. Remove the front lens. Insert a blade screwdriver under the notch at the bottom of the lens and gently pry it off.

2. Short the input signal connections and verify that the display reads zero.

3. Apply an input voltage equal to 95% of the high end of the range selected.

4. At the front panel, adjust the Span potentiometer (shown in Figure 3-2) until the display reads 19000 ±1 count.

6.2 AC VOLTAGE RANGES

1. Follow steps 1 and 2 above.

2. Apply an input voltage equal to 110.0 V ac at 50 or 60 Hz on 200 V ac range or 220 V ac at 50 or 60 Hz on 650 V ac range.

3. At the front panel, adjust the Span potentiometer (shown in Figure 3-2) until the display reads:

   110.00 on 200 V ac range

   330.0 on 650 V ac range

7.0 PARALLEL BCD OPTION (F2N)

The parallel BCD option receives serial BCD inputs from the main board and converts the data into parallel BCD for output through the rear of the unit. The data is channeled from the main board to the upper board via a 15-conductor cable and is output through the rear 50-pin card edge, P2. A mating 50-pin connector, J2, is required for BCD outputs. The J2 connector option can be mass-terminated *(D50M)* or solder-eyelet *(D50S)*.

The 2001 is shipped (standard) with internal power connection through the 15-conductor interconnect cable. To power the unit externally from the rear, open solder switch A, close solder switch B, and apply +4.7 V to P2-pin L21.

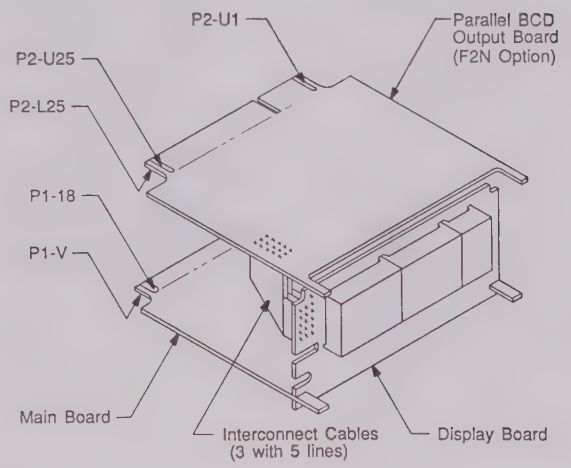


Figure 7-1 Parallel BCD Board

7.1 SPECIFICATIONS

Input Power Requirements Voltage: 4.7 V dc ±5%
Current: 10 mA

DIGITAL SIGNALS	LOGICAL 0	LOGICAL 1	I SINK	I SOURCE	IN	OUT
1. Parallel BCD 2. +Polarity 3. Overrange 4. $\overline{\text{Data Ready}}$	0 -.33 V	3.2 - 5.0 V	6 mA	6 mA		X
5. Meter Select	0 -.8 V	2.0 - 5.0 V	.8 mA	.04 mA	X	

For signals 1-4, I_O (OFF) Off-State (HI-Z state) Output Current = ±5 uA max.

7.2 SIGNAL OUTPUTS

(Three-state buffered)

Parallel BCD — TTL or 5 V CMOS compatible; outputs are stable and valid while $\overline{\text{DATA READY}}$ is low true.

+POLARITY — Logical 1 when the unit indicates a positive reading; stable when $\overline{\text{DATA READY}}$ is low true.

OVERRANGE — Logical 1 if the display is greater than ±19999; stable while $\overline{\text{DATA READY}}$ is low true.

$\overline{\text{DATA READY}}$ — Remains high for 8 milliseconds during the transfer of data into the output latches. A 5 microsecond overlap exists on leading and trailing edges of $\overline{\text{DATA READY}}$ before and after new data is updated. Therefore, both edges may be used to transfer data.

$\overline{\text{HOLD}}$ — Connects to the 2001/2001-AC $\overline{\text{HOLD}}$ input on the main board.

BCD $\overline{\text{HOLD}}$ — When input is logical 0, new BCD data is not latched when the board is enabled.

Meter Select/ Board Enable — A 4-bit address decoder allows the user to enable the instrument's parallel BCD data output with a 4-bit binary address ($\overline{B1}$ through $\overline{B8}$) for three-state data-bussing applications. The user may program the instrument with any one of sixteen 4-bit address codes by installing push-on jumpers. Refer to the parallel BCD board assembly diagram at the back of the owner's manual.

7.3 PIN ASSIGNMENTS

2001 J2 Connector

Upper		Lower	
Spare	1	1	Spare
Spare	2	2	Spare
Spare	3	3	Spare
Spare	4	4	Spare
Spare	5	5	Spare
Spare	6	6	Spare
Spare	7	7	Ground
80 k	8	8	40 k
20 k	9	9	10 k
8 k	10	10	4 k
2 k	11	11	1 k
Spare	12	12	Spare
800	13	13	400
200	14	14	100
80	15	15	40
20	16	16	10
8	17	17	4
2	18	18	1
Spare	19	19	Ground
POLARITY	20	20	$\overline{\text{DATA READY}}$
BCD $\overline{\text{HOLD}}$	21	21	+5 V dc
OVERRANGE	22	22	$\overline{\text{HOLD}}$
(address) $\overline{B8}$	23	23	$\overline{B4}$ (address)
(address) $\overline{B2}$	24	24	$\overline{B1}$ (address)
Spare	25	25	Spare

Connector pin numbers are manufacturer-dependent and must be reconciled with Newport pin locations.

Internal Cable Lead Assignments

F2N and Display Boards Interconnect Points

BCD 1	E13
BCD 2	E12
BCD 4	E2
BCD 8	E6
Digit Select 5	E9
Digit Select 4	E15
Digit Select 3	E7
Digit Select 2	E14
Digit Select 1	E8
OVERRANGE	E10
$\overline{\text{STROBE}}$	E1
+POLARITY	E11
$\overline{\text{HOLD}}$	E3
+4.7 V	E5
DIG GND	E4

Refer to Figure 8-1 for E point locations.

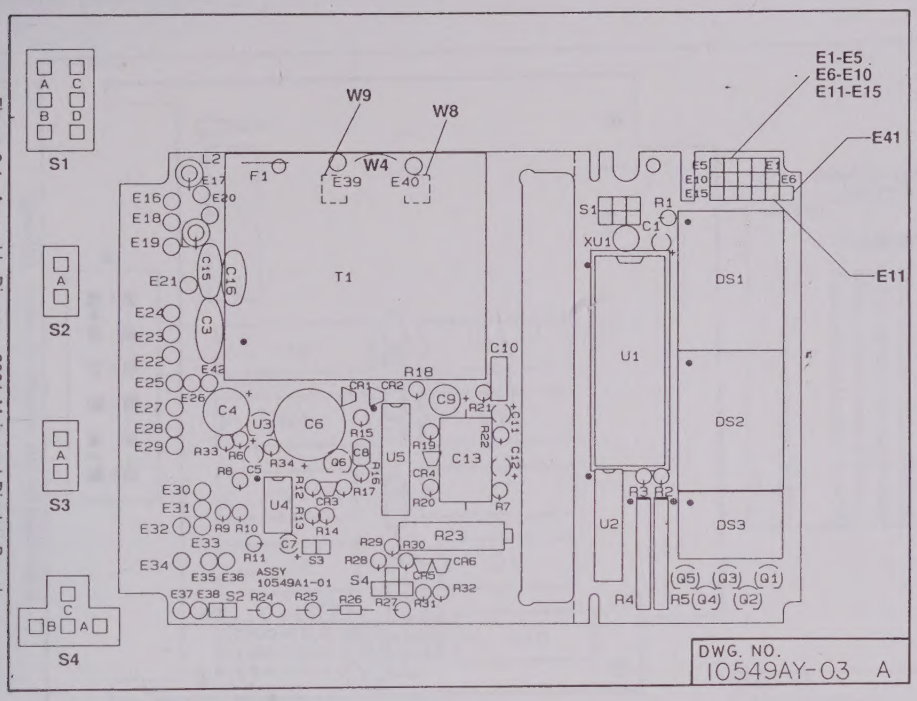


Figure 8-1 Assembly Diagram, 2001 Main and Display Board

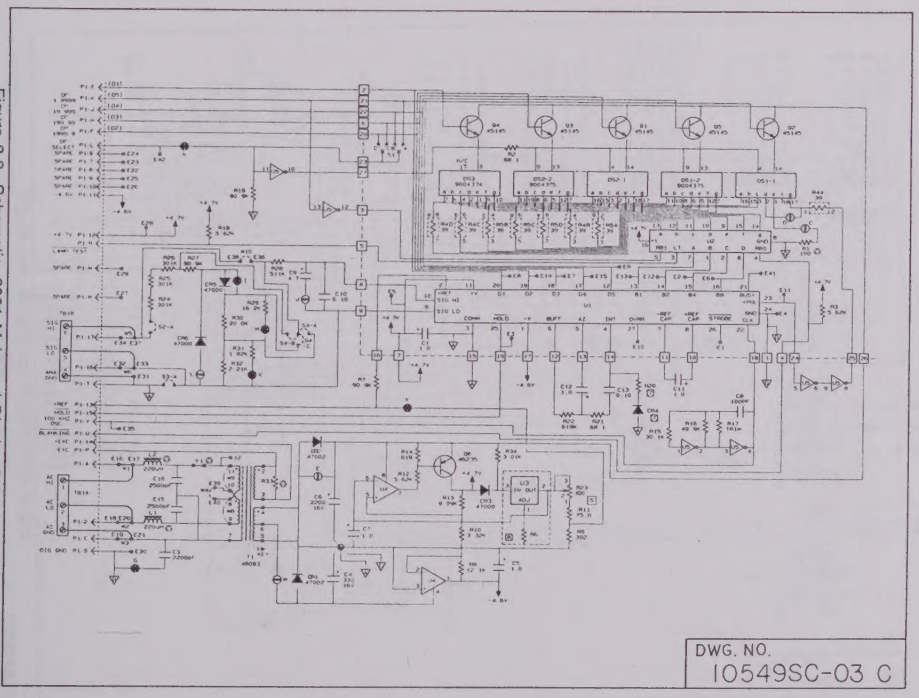
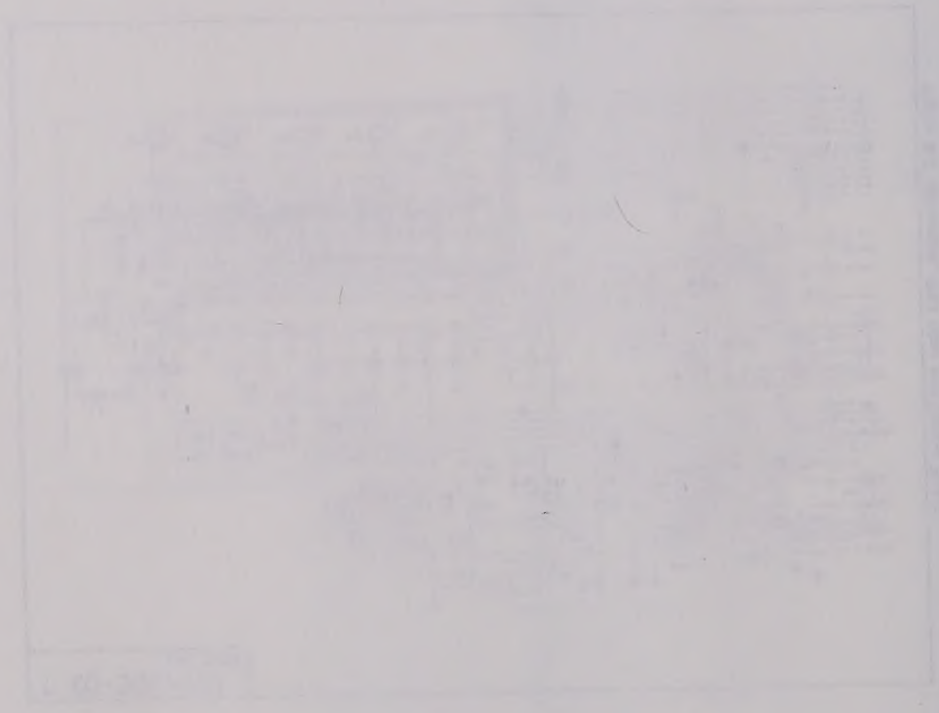
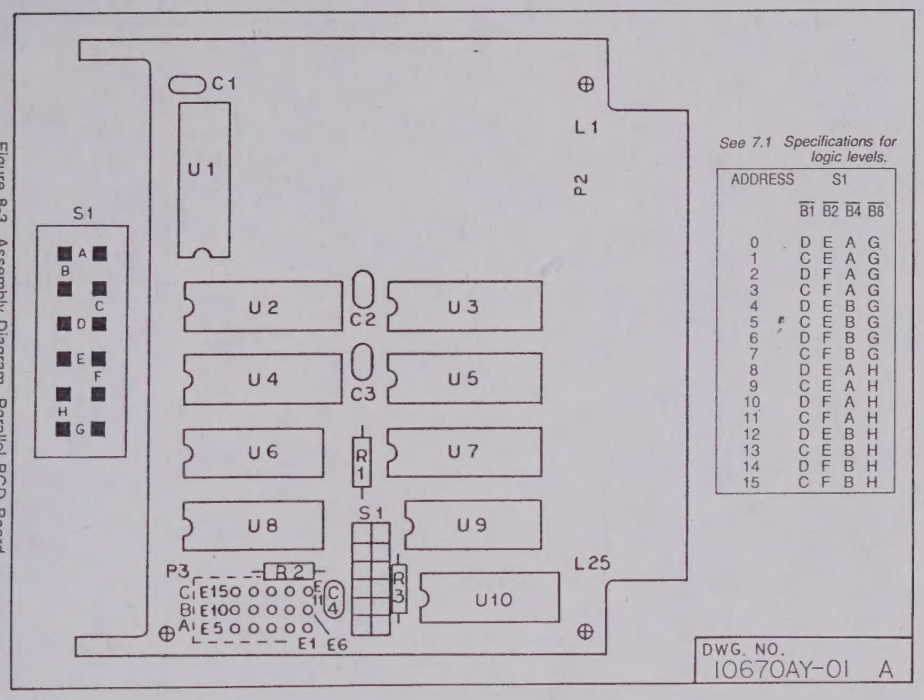


Figure 8-2 Schematic, 2001 Main and Display Board





See 7.1 Specifications for logic levels.

ADDRESS	S1			
	$\overline{B1}$	$\overline{B2}$	$\overline{B4}$	$\overline{B8}$
0	D	E	A	G
1	C	E	A	G
2	D	F	A	G
3	C	F	A	G
4	D	E	B	G
5	C	E	B	G
6	D	F	B	G
7	C	F	B	G
8	D	E	A	H
9	C	E	A	H
10	D	F	A	H
11	C	F	A	H
12	D	E	B	H
13	C	E	B	H
14	D	F	B	H
15	C	F	B	H

Figure 8-3 Assembly Diagram, Parallel BCD Board
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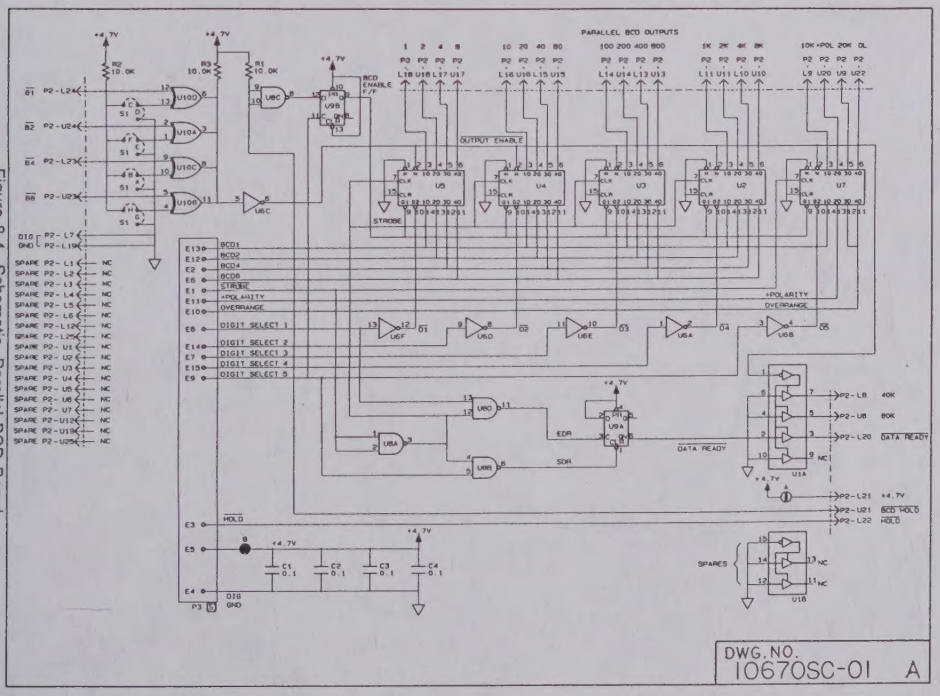

Figure 8-4 Schematic, Parallel BCD Board
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